Investigation of a Low-Power LDO Regulator with Rapid Transient Response

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**Abstract.** The growing demand for energy-efficient and high-performance portable electronic devices has driven advancements in power management solutions, particularly in low-dropout (LDO) linear regulators. To address the dual challenges of low power consumption and swift transient response, this review focuses on LDO regulators employing adaptive-bias techniques. By dynamically tuning the bias current and circuit topology, these regulators achieve nanoampere-level quiescent current under light loads while enhancing loop gain and drive strength during heavy loads, striking an optimal balance between efficiency and transient performance. Key methods explored include dynamic bias-current mapping, power-transistor bank switching, subthreshold-region optimization, and adaptive feedback compensation, all of which significantly suppress voltage overshoot and undershoot while reducing recovery time. Additionally, multi-stage compensation strategies—such as dynamic feedback-resistor networks, push–pull buffering, and transient assistance paths—are examined. These approaches enable low quiescent current without sacrificing transient response, offering a comprehensive power-management solution that combines ultra-low standby consumption with rapid transient performance.

# introduction

With the rapid growth of portable electronic devices such as smartphones, laptops, and tablets, the demand for high-performance power supplies has significantly increased. Key requirements include low power consumption, minimal noise, and compact size.Currently, mainstream power management integrated circuits (ICs) can be categorized into three types based on their operating principles: switching DC–DC converters, charge pumps, and low-dropout (LDO) linear regulators [1].DC–DC converters are compact but suffer from low efficiency. Charge pumps are cost-effective but have limited efficiency and are susceptible to electromagnetic interference.Among linear regulators, low-dropout (LDO) regulators are the most commonly used. They are widely adopted in low-voltage, low-power systems due to their simple architecture, low power consumption, minimal ripple, and low noise.

With the rapid development of portable devices, improving energy efficiency has become a critical challenge in battery management systems. Low-power LDOs optimize circuit architecture and operating modes to significantly reduce standby power consumption, effectively extending device battery life. This advantage has made them a focus of current research in power management ICs.

The rapid growth of emerging fields such as IoT, wearable devices, and automotive electronics has raised the bar for LDO transient response. For instance, IoT nodes must quickly respond to sudden operational demands from peripherals like sensors during prolonged operation, while the activation and deactivation of modules in wearable devices can induce transient load current changes. These scenarios demand that LDOs accurately and promptly react to load current variations within a short timeframe to ensure proper device operation. As a result, fast transient response has become a key research parameter for LDOs.

Low-power design is typically achieved by reducing quiescent current, but this may cause the transistors within the LDO to operate in the subthreshold or weak inversion region, thereby increasing their on-resistance. On the other hand, transient response requires the LDO to rapidly react to changes in load current, necessitating a high driving current to adjust the output voltage quickly. These demands conflict with the principles of low-power circuit design, making the trade-off between low power consumption and transient response a key area of research. This paper analyzes adaptive bias circuits employing dynamic bias current mapping, power transistor segmentation, subthreshold region optimization, and dynamic feedback compensation. It also reviews multi-stage compensation strategies, including dynamic feedback resistors, push-pull buffers, and transient auxiliary paths, which enable improved transient response while maintaining low power consumption.

# The Fundamental Principles of LDO



**FIGURE 1.** Basic Structure of LDO

As a direct current voltage regulator, the Low-Dropout Regulator (LDO) comprises core components including the error amplifier, power pass transistor, resistive voltage divider feedback network, and voltage reference source. The overall architecture is illustrated in Figure 1. Auxiliary circuits are designed to enhance system reliability and improve the stability and response speed of the feedback loop under transient conditions. The voltage reference source generates a temperature-stable reference voltage, . This reference voltage is compared with the feedback voltage, obtained from the feedback network through the error amplifier. The resulting output signal drives the gate of the power transistor, modulating its conduction resistance to precisely control the output voltage, When the input voltage fluctuates or the load resistance, Rout, changes, the closed-loop system formed by the error amplifier, PMOS power transistor, and feedback network dynamically adjusts the operating state of the power transistor to maintain a stable output voltage[2].

# Adaptive Bias Circuit

## Adaptive Power Transistor and Dynamic Structural Switching

A method proposed by researchers from Nanyang Technological University, Singapore, involves dynamically switching the gain stages of an LDO based on the load current to avoid redundant power consumption during light load conditions. The power transistors are grouped into auxiliary and main power transistors. Under light load, the LDO operates in a two-stage mode comprising the error amplifier and the auxiliary power transistor; with the main power transistor turned off, only the error amplifier and a non-inverting amplifier drive the auxiliary power transistor. At this time, the non-inverting amplifier operates in the active (triode) region, achieving low gain and low power consumption. Under heavy load, the circuit switches to a three-stage topology consisting of the error amplifier, non-inverting amplifier, and main power transistor. When the load current exceeds a threshold, the non-inverting amplifier enters saturation, achieving high gain and activating the main power transistor to provide sufficient driving capability [3]. This approach combines dynamic gain-stage switching with coordinated control of transistor grouping and amplifier operating regions to achieve a dynamic balance between power efficiency and driving capability. Additionally, by time-sharing the main and auxiliary power transistors, it overcomes the limitations of traditional fixed-topology LDOs, ensuring stable output voltage while further reducing power consumption.

## Adaptive Current Technique

This method employs a comparator circuit to achieve precise threshold triggering. When the circuit is unloaded or lightly loaded, the adaptive bias branch is completely shut off, retaining only a minimal static current path, thereby significantly reducing power consumption. Under load conditions, the load current is detected via a sampling transistor; combined with feedback signals, the switch is rapidly activated to initiate a large bias current. This enhances the driving capability of the error amplifier and accelerates transient response. Compared to traditional adaptive bias circuits, this approach can fully disable the adaptive bias circuit during no-load or light-load conditions, resulting in lower static current and thus reduced power consumption. Its innovative dual-path feedback architecture deeply integrates load state sensing with loop response, maintaining an ultra-low static current profile while providing the system with sensitive load-tracking capability [1].

## Comparison between Dynamic Bias and Adaptive Bias Methods

Both dynamic bias and adaptive bias methods are commonly used approaches for tail current biasing in error amplifiers. Dynamic bias optimizes performance by adaptively adjusting the bias current of the error amplifier. This method establishes a dynamic bias coupling mechanism to regulate key parameters. It effectively suppresses voltage overshoot and undershoot during load changes while dynamically controlling the gate voltage of the power transistor. Consequently, it shortens recovery time and improves response speed [4]. However, the bias current remains constant during steady-state operation and only temporarily increases during transient load responses, lacking compensation for long-term parameter drift. In contrast, adaptive bias employs closed-loop control to proportionally vary the bias current with the load current. Under increased load conditions, the bias circuit automatically enhances the operating current, achieving synergistic optimization of transconductance gain and frequency response [2].

# Subthreshold Current Biasing

In low-power circuit design, adopting subthreshold operation technology has become an effective approach to optimize static power consumption. Specifically, some compensation circuits and adaptive bias modules can achieve significant energy savings by appropriately biasing into the subthreshold region. For example, when an error amplifier employs subthreshold biasing, its core differential pair operates in the subthreshold region, leveraging the high transconductance efficiency of this area to achieve high gain at nanoampere-level currents without increasing current to enhance transconductance. This mechanism maintains loop gain while effectively avoiding the positive correlation between gain and power consumption seen in traditional strong inversion designs.

Another key advantage of subthreshold design lies in its potential applications in voltage reference circuits. These circuits can effectively achieve temperature compensation by combining components with different temperature characteristics. Research has shown that leveraging the properties of subthreshold MOSFETs enables the design of highly stable and efficient voltage reference circuits[5]. By properly configuring the temperature characteristics and biasing modes of the devices, these circuits can maintain output voltage stability while achieving low power consumption, catering to modern low-power applications such as portable devices and IoT terminals. This approach not only reduces power consumption but also demonstrates significant advantages in temperature compensation and process adaptability.

Furthermore, a notable feature of subthreshold technology is its ability to significantly reduce static current. When power transistors operate in the subthreshold region, their static power consumption approaches the theoretical minimum, with leakage current significantly reduced under no-load conditions. While this design involves certain trade-offs in transconductance performance, adjustments to device geometries, such as width-to-length ratios, can balance power consumption and performance. This strategy offers unparalleled benefits in scenarios requiring ultra-low static power consumption.

It is worth noting that subthreshold technology is highly sensitive to process variations, necessitating optimization through process compensation techniques. Studies have shown that adaptive body biasing and dynamic threshold adjustment are effective solutions, significantly enhancing circuit robustness and stability[5]. This combined technological approach not only suppresses process corner effects and temperature drift but also expands the applicability of subthreshold circuits.

In conclusion, subthreshold operation technology provides innovative ideas for low-power circuit design and demonstrates unique advantages in voltage reference circuits, power transistor optimization, and process compensation design. By deeply integrating this technology with modern process technologies, its widespread application prospects in low-power electronic systems are highly promising.

# Design of Low-Static-Current Error Amplifiers

## Cross-Coupled Error Amplifier

The cross-coupled architecture significantly enhances the effective transconductance at low bias currents through the synergistic effects of positive and negative feedback, achieving higher gain under the same current conditions. In a low-power circuit designed by Xie Haiqing et al., the second stage of the error amplifier adopts a self-biased common-source common-gate configuration. By leveraging the current mirror characteristics of the cascaded transistors, the bias current of the first stage is reused, eliminating the need for additional bias circuits and reducing static current branches. Simultaneously, the high output impedance of the common-source common-gate structure directly boosts gain without increasing tail current [6]. This design not only improves the gain-to-power ratio but also reduces circuit complexity through topology optimization, representing a significant engineering innovation.

## Operational Transconductance Amplifier (OTA)-Based Error Amplifier

Young-li Kim proposed a low-power error amplifier design method based on the synergistic optimization of an AB-class dynamic transconductance architecture and adaptive biasing. The core concept leverages the hybrid operation mode of an AB-class operational transconductance amplifier (OTA) to maintain ultra-low quiescent current under static conditions, while achieving transconductance multiplication during transient response through parallel summation of transconductance paths. Combined with a flipped voltage follower (FVF) dynamic tail current regulation mechanism, this design establishes a dual-mode biasing system of "static subthreshold - dynamic strong inversion." In steady-state operation, the system employs the minimum necessary bias current to reduce power consumption. Upon detecting load transients, dynamic current injection is triggered via voltage follower detection within a pseudo-differential structure, enabling adaptive enhancement of transconductance gain and driving capability. Furthermore, coupled transient voltage spike detection technology utilizes the coupling effect of compensation capacitors to create a fast response path, allowing the system to maintain microampere-level quiescent power consumption while achieving a settling time six times faster and 385 mV transient suppression compared to conventional architectures [7]. This dynamic energy efficiency conversion mechanism, through circuit topology innovation, breaks the traditional power-bandwidth trade-off in LDOs, offering a new design paradigm for high-efficiency power management chips.

# Circuit Optimization for Enhanced Transient Response

## Dynamic Feedback Resistor

The dynamic feedback resistor mechanism is an innovative design that optimizes the transient performance of capacitor-less low-dropout regulators by dynamically adjusting the feedback loop impedance in real time. Its core principle involves employing variable impedance elements to sense transient changes in the output voltage and dynamically adjusting the resistance in the feedback path to enable rapid response. When the output voltage undershoots, the feedback resistance momentarily increases to reduce feedback current, accelerating the discharge of the output node; conversely, during overshoot, the resistance decreases to increase feedback current, suppressing voltage rise. This mechanism eliminates the need for external capacitors or complex detection circuits, directly achieving dynamic loop bandwidth expansion through an integrated feedback network [8]. Working synergistically with adaptive biased power transistor architectures, it enables low quiescent current, high stability, and excellent transient performance without external capacitors, making it particularly suitable for power management in portable devices with stringent power and area constraints.

## Push-Pull Buffer

In LDOs, the push-pull buffer dynamically adjusts the charging and discharging paths of the power transistor gate using complementary transistors. The core design concept leverages an asymmetric current enhancement mechanism for transient response. This structure maintains ultra-low static current during steady-state operation but significantly boosts the gate node's charging and discharging capability during load transients by dynamically activating complementary drive branches, thereby overcoming the speed limitations of traditional feedback loops [9]. Its innovation lies in two aspects: first, it uses a source follower to achieve impedance matching for control signals, avoiding the introduction of additional high-frequency poles while enhancing transient drive capability; second, it works synergistically with an adaptive compensation network to achieve stability across a wide load range without external capacitors. However, the design is sensitive to transistor matching, may be influenced by parasitic parameters at high frequencies, and is subject to symmetry constraints in transient response due to process variations. From a methodological perspective, this dynamic local enhancement strategy provides an efficient optimization pathway for low-power analog circuits. Future integration with adaptive biasing or process calibration techniques holds promise for improved robustness。

## Dynamic Current Compensation

A research team from the School of Electronic Engineering at Xi'an University of Technology has proposed a novel capacitor-less LDO architecture, with its core innovation lying in the implementation of a "primary error loop + dual transient auxiliary loops" collaborative control mechanism.This design employs output voltage rate-of-change detection to activate dual transient enhancement circuits, creating a rapid charge regulation pathway independent of the traditional error amplifier. During load transients, it directly drives the gate of the power transistor and facilitates charge redistribution at the output node.Leveraging a dynamic detection mechanism and dual-path compensation strategy, this design effectively suppresses output voltage fluctuations during load transients in scenarios with load changes of tens of milliamps. It not only mitigates transient overshoot and undershoot but also compresses voltage recovery time to the microsecond range through a cross-tier charge redistribution mechanism, achieving significantly improved transient response performance compared to traditional architectures.To balance system stability and bandwidth optimization, the research team adopted a single-stage folded cascode error amplifier combined with multi-stage pole compensation techniques. By implementing a dynamic separation strategy for primary and secondary poles, the design ensures adequate phase margin across the full load range while intelligently extending loop bandwidth.This architecture offers a new design paradigm for enhancing the transient performance of capacitor-less LDOs, and its core principles provide significant insights for the design of power management chips requiring high dynamic response capabilities[10].

# Conclusion

This paper systematically investigates the design of a low-power, fast transient response LDO regulator based on adaptive biasing techniques. Addressing the stringent dual demands of portable electronic devices on static power consumption and dynamic performance, a series of key technologies and optimization strategies are proposed. By dynamically adjusting the bias current, employing power transistor grouping switching, optimizing subthreshold operation, and implementing dynamic feedback compensation mechanisms, the design achieves nanoampere-level quiescent current under light load conditions while effectively balancing loop gain and driving capability under heavy load conditions, significantly enhancing transient response performance. The study shows that the adaptive bias circuit dynamically adjusts the biasing states of the error amplifier and power transistor through load current mapping, effectively suppressing output voltage overshoot and undershoot, shortening recovery time, and improving system stability and response speed.

Furthermore, this paper reviews circuit designs operating in the subthreshold region, which effectively reduce static power consumption while optimizing the trade-off between transconductance gain and power consumption by rational device sizing and biasing. Combined with low-static-error amplifier designs and multi-stage compensation techniques—such as dynamic feedback resistors, push-pull buffers, and dual-loop compensation—this approach overcomes the traditional contradiction between power consumption and transient response in LDO design, providing feasible solutions for high-performance power management without external capacitors.

Looking forward, as portable devices, IoT, wearable electronics, and automotive electronics increasingly demand higher performance from power management ICs, low-power fast transient response LDO designs will face more stringent challenges. Future research should further integrate advanced semiconductor processes, intelligent control algorithms, and innovative circuit architectures to improve the precision and robustness of dynamic bias current adjustment, enhance compensation for process parameter variations, and optimize system stability and energy efficiency. Meanwhile, incorporating AI-assisted design and on-chip adaptive tuning technologies holds promise for realizing more intelligent, flexible, and efficient LDO solutions, driving their critical role in broader application domains and industrialization progress.

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